AMENDMENTS TO THE SPECIFICATION

Please amend the following paragraph:

[0039] FIG. 7 also illustrates the remaining devices of the pixel 100, including respective source/drain regions 140, 141, 142 of the source follower and row select transistors 136, 138 formed on either sides of their respective gate stacks and within a p-type heavily doped well 121 by well-known implantation methods. Regions 121, 140, 141 and 142 may be formed at an earlier stage of fabrication, if desired. Conventional processing steps may be also employed to form contacts and wiring 137 to connect the gate of source follower transistor to contact region 177, and to connect capacitor 171 to contact region 177. For example, the entire substrate surface may be covered with a passivation layer of, e.g., silicon dioxide, BSG, PSG, or BPSG, which is CMP planarized and etched to provide contact holes, which are then metallized to provide contacts to the contact region 177, gate 136a of the source follower transistor (via conductor [[131]] 137) and to voltage source Vdd. Conventional multiple layers of conductors and insulators to other circuit structures may also be used to interconnect the internal structures of the pixel cell and to connect the pixel cell structures to other circuitry associated with a pixel array.